Amendments to the Claims

Please amend Claim 46. Please cancel Claims 47-48 and 50. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1-45. (Canceled)

46. (Currently Amended) A ~~queuing~~ method of processing data packets in a switch comprising the steps of:

receiving data packets on an ingress port of the switch and writing the data packets to buffer memory of the switch;

writing in a first memory of an egress port of the switch, ~~having a first memory access time,~~ a plurality of pointers pointing to the data packets in the buffer memory, the first memory having a first memory access time; ~~and~~

establishing a linked list by transferring, in a single transfer cycle, the plurality of pointers to a second memory of the egress port, the second memory having a second memory access time that is significantly slower than the first memory access time; and

dequeuing each pointer from the second memory and forwarding the corresponding data packet from the egress port.

47. (Canceled)

48. (Canceled)

49. (Previously Presented) A queuing method as claimed in Claim 46 wherein the step of writing writes each pointer in a single write operation to the first memory.

50. (Canceled)

51. (Previously Presented) A queuing method as claimed in Claim 46 wherein the step of transferring forwards a full cache row into the second memory.

52. (Previously Presented) A queuing method as claimed in Claim 46 wherein the step of transferring forwards a partially filled cache row into the second memory.

53. (Previously Presented) A queuing method as claimed in Claim 51 wherein the cache row is transferred in a single write cycle.

54. (Previously Presented) A queuing method as claimed in Claim 52 wherein the cache row is transferred in single write cycle.

55. (Previously Presented) A queuing method as claimed in Claim 46 wherein entries in a cache row in first memory are ordered by position in the cache row.

56. (Previously Presented) A queuing method as claimed in Claim 46 wherein the first memory includes two cache rows.

57. (Previously Presented) A queuing method as claimed in Claim 46 wherein a packet vector stored in the second memory includes a cache row and a count of the number of pointers stored in the cache row.

58. (Previously Presented) A queuing method as claimed in Claim 46 wherein a packet vector stored in the second memory includes a link to a next packet vector.

59. (Previously Presented) A queuing method as claimed in Claim 57 wherein a packet vector stored in the second memory includes a link to a next packet vector.

60. (Previously Presented) A queuing method as claimed in Claim 46 wherein the plurality of pointers are packet pointers.

61. (Previously Presented) A queuing method as claimed in Claim 46 wherein at least one of the plurality of pointers is written into an egress port queue.

62. (Previously Presented) A queuing method as claimed in Claim 46 wherein each pointer is determined from a packet header of a data packet.